# Low Standby Power Offline Switching Power IC

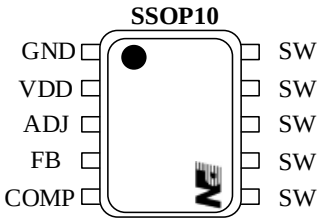
## General description

The PN8085 consists of an integrated Current Mode Modulator controller and power MOSFET, specifically designed for a high performance off-line converter with minimal external components.

PWM, Burst-mode operation and low consumption device help to meet the standby energy saving standards and achieve higher efficiency. PN8085 can be designed for non-isolated flyback and Buck applications to meet different application requirements. Frequency modulation technology and Soft Driver technology fully guarantee good EMI performance.

The PN8085 offers complete protections including output over voltage protection, Cycle-by-Cycle current limiting (adjustable OCP), and OLP, and soft-start etc.

## Package/Order Information




| Order code | Package | Typical Power |
|---|---|---|
| | | 85~265$V_{AC}$ |
| PN8085ST-A1 | SSOP10 | 5W |
| PN8085LST-A1 | SSOP10 | 5W |
| PN8085HST-A1 | SSOP10 | 5W |

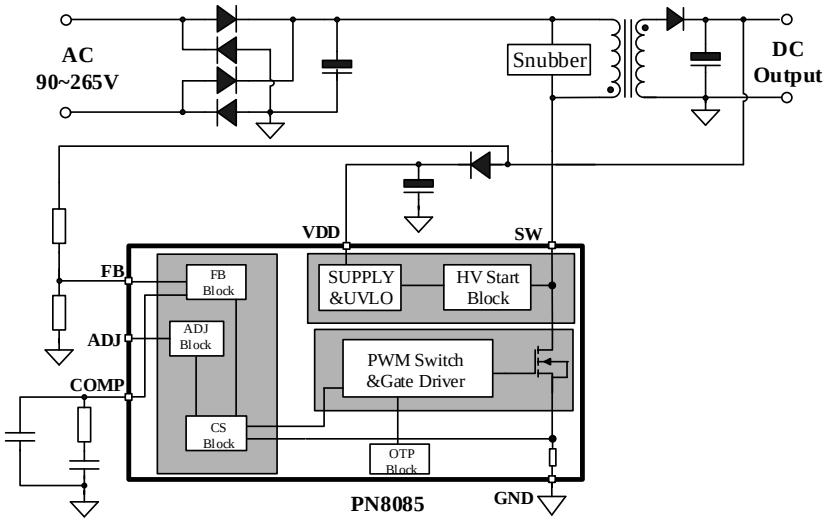
## Features

- Internal 800V avalanche-rugged smart power VDMOSFET
- Non-isolated flyback and Buck applications PWM, Burst-mode
- Without startup resistance and CS detection resistance
- Internal HV Start-up Circuit, High and low voltage pin arranged on both sides to improve safety
- No-load consumption power < 30mW @230VAC
- Frequency modulation for low EMI
- VDD Operating voltage range 9~23V
- Excellent Protection Coverage:
  - ✧ Over Temperature Protection (OTP)
  - ✧ VDD Over Voltage Protection(OVP)
  - ✧ Cycle-by-Cycle Current Limiting (OCP)
  - ✧ Over load Protection(OLP)

## Application

- Standby power supply
- Switch AC/DC
- White goods box power supply

## Typical Circuit



## Pin Definitions

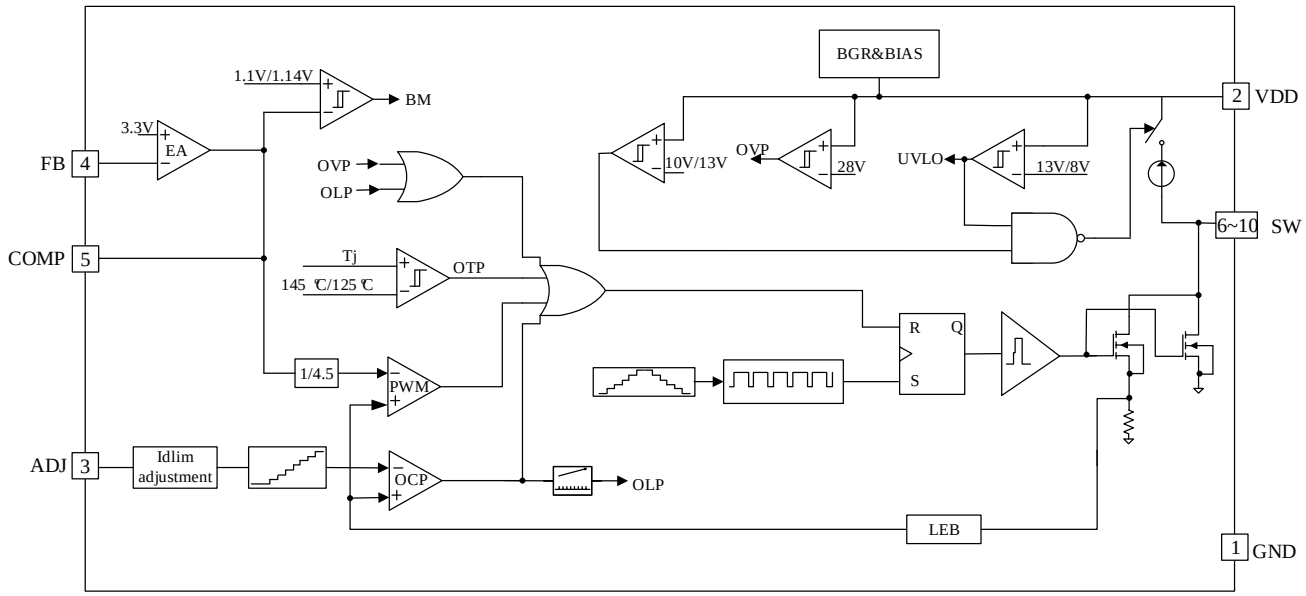
| Pin Name | Pin Number | Pin Function Description |
|---|---|---|
| GND | 1 | Ground |
| VDD | 2 | Power supply pin |
| ADJ | 3 | The overcurrent point is adjusted by the grounding resistance |
| FB | 4 | Flyback input pin |
| COMP | 5 | Error amplifier compensation |
| SW | 6,7,8,9,10 | Drain of the internal MOSFET |

## Typical Power

| Part Number | Input Voltage | Adaptor(1) | Open Frame(2) |
|---|---|---|---|
| PN8085 | 85~265$V_{AC}$ | 4W | 5W |
| | 230$V_{AC}$ | 6W | 8W |

Note:
1. Typical practical continuous power is measured in closed environment at 50℃ ambient temperature.
2. Typical practical continuous power is measured in opened environment at 50℃ ambient temperature.

## Block Diagram



## Absolute Maximum Ratings

Supply voltage Pin VDD……-0.3~33V
Pin FB,ADJ,COMP……-0.3~6.5V
High-Voltage Pin, SW ……..…….. -0.3~800V
Operating Junction Temperature……..…-40~150℃
Storage Temperature Range……..-55~150℃

Lead Temperature (Soldering, 10Secs)……..…260℃
Package Thermal Resistance $\theta_{JC}$ (SSOP10)……..40℃/W
HBM ESD Protection [1]…..……..…… ±2kV
Pulse Drain Current ($T_{pulse}$=100us)……2A

Note:
1. Test standard: ANSI/ESDA/JEDEC JS-001-2017.

## Electrical Characteristics

($T_A$= 25℃, unless otherwise specified)

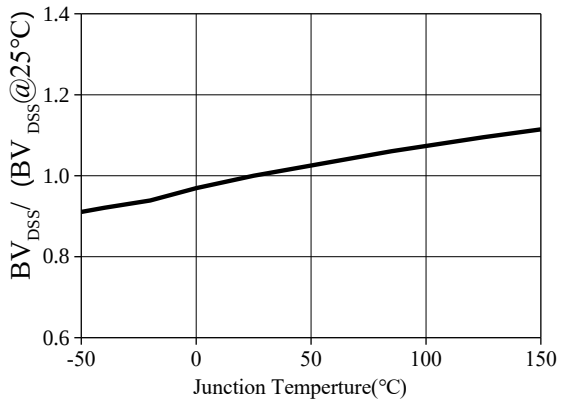
| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Power Section** | | | | | | |
| Break-down voltage | $BV_{DSS}$ | $I_{SW}$ =250uA, $T_J$ =25℃ | 800 | 820 | | V |
| Off-state drain current | $I_{OFF}$ | $V_{SW}$ =650V, $T_J$ =25℃ | | | 100 | uA |
| Drain-source on state resistance | $R_{DS(on)}$ | $I_{SW}$ = 400mA, $T_J$ =25℃ | | 19 | | Ω |
| **Supply Voltage Section** | | | | | | |
| VDD start up threshold | $VDD_{on}$ | | 12 | 13 | 14 | V |
| VDD under voltage shutdown threshold | $VDD_{off}$ | | 7 | 8 | 9 | V |
| $V_{DD}$ clamp voltage | $V_{CLAMP}$ | | 23 | 24.5 | 26 | V |
| VDD over voltage protect | $VDD_{ovp}$ | | 26.5 | 28 | 29.5 | V |
| VDD self-powered charging voltage | $VDD_{RECH}$ | | 8.5 | 9.7 | 11 | V |
| Time between restarts after protection | $T_{RST}$ | | | 1.1 | | s |
| Drain-source startup voltage | $V_{DRAIN\_START}$ | | 25 | | 45 | V |
| **Supply Current Section** | | | | | | |
| Start up charging current | $I_{VDD\_CH}$ | | | -1.2 | | mA |
| self-powered charging current | $I_{VDD\_RECH}$ | | | -9 | | mA |
| Operating supply current, switching | $I_{VDD0}$ | $V_{FB}$=3.5V | | 1 | 1.5 | mA |
| Operating supply current, under burst mode | $I_{VDD1}$ | $V_{FB}$=0.5V | | 0.5 | 0.75 | mA |
| Operating supply current, with protection tripping | $I_{VDD\_Fault}$ | | | 0.6 | 0.9 | mA |
| **Oscillator Section** | | | | | | |
| Switching Frequency - PN8085 | $F_{OSC}$ | | | 30 | | kHz |
| Switching Frequency - PN8085L | | | | 60 | | kHz |
| Switching Frequency - PN8085H | | | | 115 | | kHz |
| Maximum duty cycle | $D_{MAX}$ | | 75 | 80 | 85 | % |
| Modulation frequency | FM | | | 230 | | Hz |
| Frequency Variation | FD | | | ±7 | | % |

## Electrical Characteristics

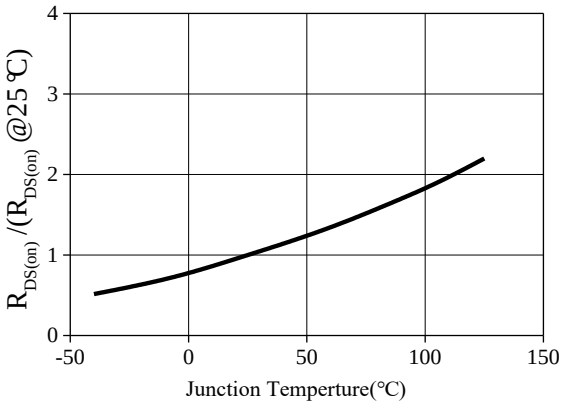
($T_A$= 25℃, unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **FB Section** | | | | | | |
| EA reference voltage | $V_{REF\_EA}$ | | 3.2 | 3.3 | 3.4 | V |
| FB pull on current | $I_{FB\_PULL}$ | | | 1 | | uA |
| Trans conductance | Gm | | | 2 | | mA/V |
| **Error Amplifier Compensation Section** | | | | | | |
| $V_{COMP\ open}$ Loop Voltage | $V_{COMP\_OPEN}$ | | | 5 | | V |
| COMP sink/source current | $I_{COMP1}$ | | | 0.15 | | mA |
| COMP short circuit current | $I_{COMP2}$ | | | 0.21 | | mA |
| Intermittent mode threshold voltage | $V_{COMP\_BM\_H}$ | | | 1.1 | | V |
| Intermittent mode hysteresis voltage | $V_{COMP\_BM\_HYS}$ | | | 40 | | mV |
| COMP impedance | $R_{COMP}$ | | | 25 | | kΩ |
| **Current Sense Section** | | | | | | |
| Soft-start time | Tss | | | 7.5 | | ms |
| Leading edge blanking time | $T_{LEB}$ | | | 450 | | ns |
| Drain current limit time | $ID_{LIM}$ | | 0.32 | 0.35 | 0.38 | A |
| OCP blanking time | Td_OCP | | | 50 | | ms |
| Burst-mode drain current | ID_BM | | | 0.085 | | A |
| **Adjust Section** | | | | | | |
| ADJ open-circuit voltage | $V_{ADJ\_OPEN}$ | | | 2 | | V |
| ADJ clamping voltage | $V_{ADJ\_CLP}$ | | | 0.5 | | V |
| **Thermal Section** | | | | | | |
| Thermal shutdown temperature | $T_{SD}$ | | 135 | 145 | | ℃ |
| Thermal shutdown hysteresis | $T_{HYST}$ | | | 20 | | ℃ |

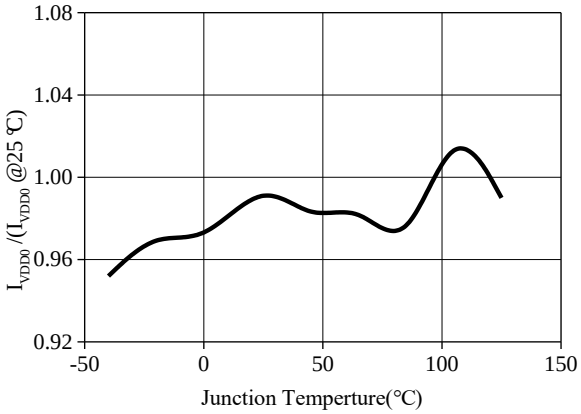
## Typical Characteristics Plots



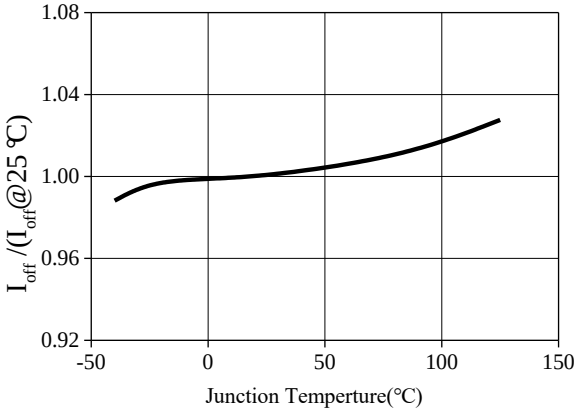

(a) $BV_{DSS}$ VS $T_j$



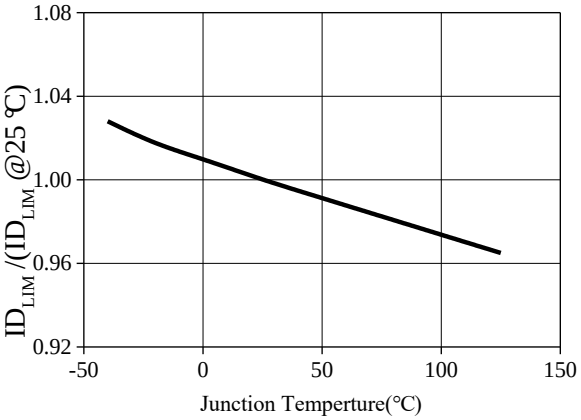

(b) $R_{DS(on)}$ VS $T_j$




(c) $I_{VDD0}$ VS $T_j$




(d) $I_{off}$ VS $T_j$




(e)$ID_{LIM}$ VS $T_j$

# Functional Description

## 1. Startup

At start up, the internal high-voltage current source supplies the internal bias and charges the external VDD capacitor. When VDD reaches $VDD_{on}$, the device starts switching and the internal high-voltage current source stops charging the capacitor. After start up, the output to the VDD capacitor can be used to provide energy.

## 2. Soft-start up

In the process of startup, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and prevent the transformer turning into the saturation state. Typically, the duration of soft-start is 7.5ms.

## 3. Error Amplifier

The PN8085 internal integrated error amplifier samples the output voltage through the FB pin, and the FB pin voltage compares to the internal reference 3.3V (typical value). $V_{COMP}$ is the voltage after error amplification, COMP needs an external compensation circuit to prevent loop oscillation.

## 4. Over current protection threshold adjustment

For some applications, $ID_{LIM}$ may lead to high system overload protection power. In the case, $ID_{LIM}$ can be reduced by adjust external resistance to the ground to match the requirements of the system.

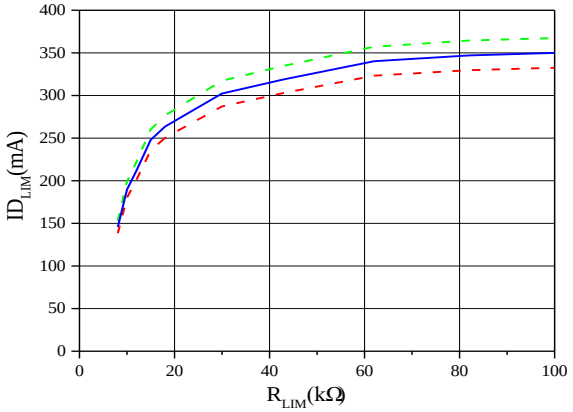



Fig.1 $ID_{LIM}$ adjustment

## 5. Multi-mode work

PN8085 integrates PWM and burst-mode mixed modulation technologies to achieve ultra-low standby power consumption and the best efficiency in the full voltage rang.

At full load, PN8085 operates in PWM mode with a fixed oscillation frequency, and the operating frequency is Fosc.

The PN8085 enters burst-mode operation in order to minimize the power dissipation in standby mode. As the load decreases, the feedback voltage decreases. When the voltage on comp pin falls below $V_{COMP\_BM\_L}$, the device enters burst mode and power MOSFET stops switching. It can be switched on again once the voltage on COMP pin exceeds $V_{COMP\_BM}+V_{COMP\_BM\_HYS}$.

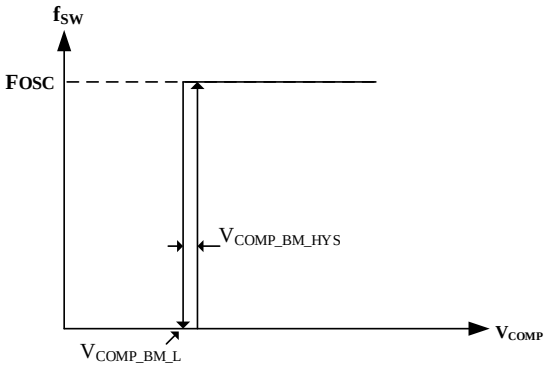



Fig.2 $F_{OSC}$ VS $V_{comp}$

## 6. Over load protection (OLP)

Over load is defined as the load current exceeding a pre-set level due to an accident event as a fault. MOSFET current is the over-current protection threshold and meets the delay time of 50ms, the overload protection is triggered.

## 7. Over temperature protection (OTP)

The power MOSFET and control chip are integrated, making it easier for control chip to detect the temperature of MOSFET. If the temperature exceeds about 145℃, OTP fault is activated. OTP is self-recovered when the temperature falls below 125℃.

## 8. Error state timing self-recovery function

When VDD overvoltage, overload protection or over temperature protection occurs on the chip, PWM will turn off for 1.1s, VDD will open the self-supply circuit to maintain VDD voltage. After 1.1s, PN8085 redetects whether the error state is resolved. By shutting down the system for 1S after the error state, the power consumption of the error state can be effectively reduced.

## 9. Gate driver

The internal power MOSFET in PN8085 driven by a dedicated gate driver for power switch control. A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time. The good EMI system design and low idle loss is easier to achieve with this dedicated control scheme.

## Typical Application

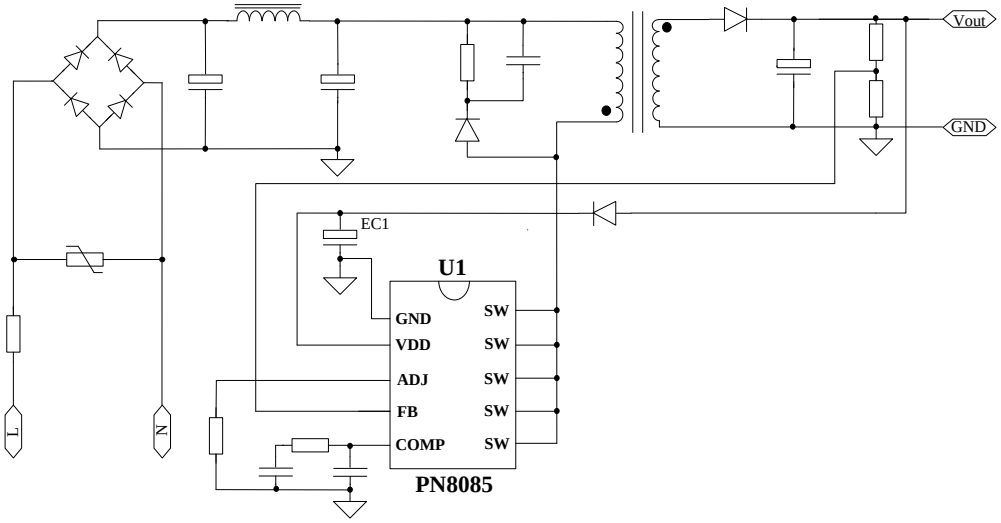



Fig.3 non-isolated fiyback application

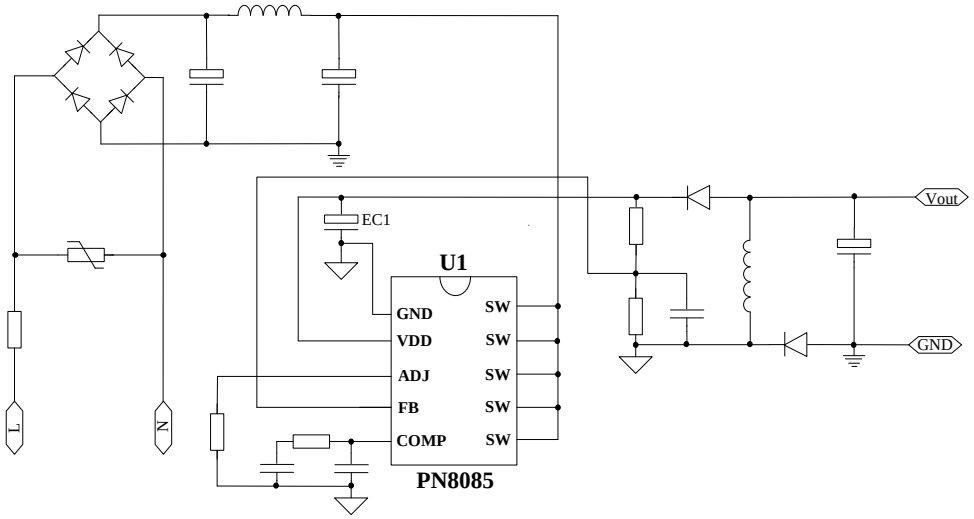


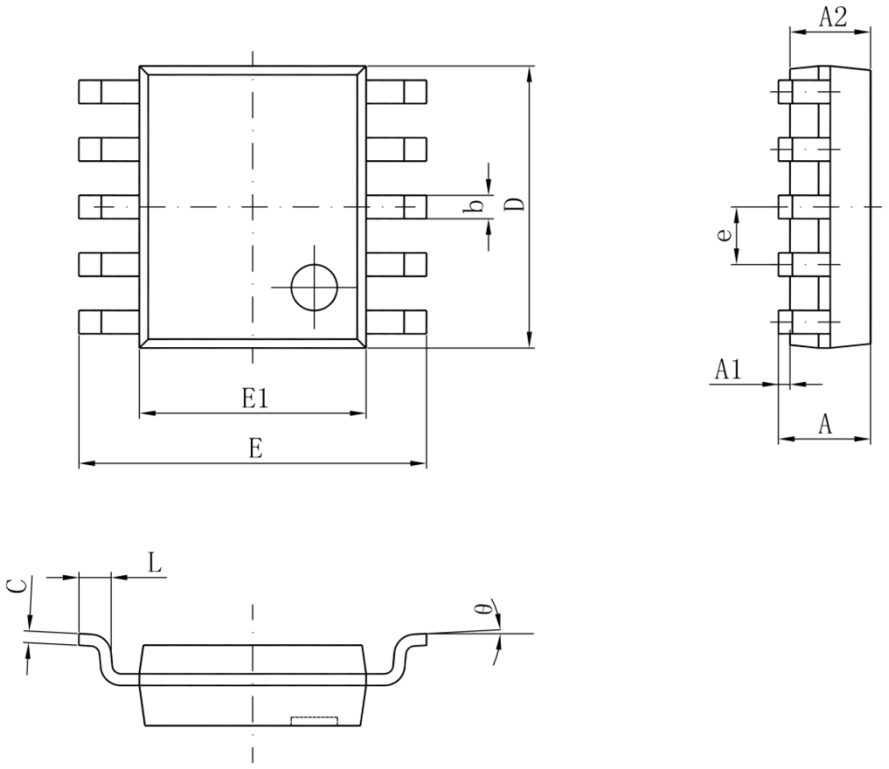

Fig.4 Buck system

## Component Parameter and Layout Considerations:

1. VDD capacitor EC1 should be placed at the nearest place between the VDD pin and the GND pin.
2. The line from PN8085 GND pin to the input electrolytic capacitor need to as short as possible

# Package Information

## Package Information SSOP10



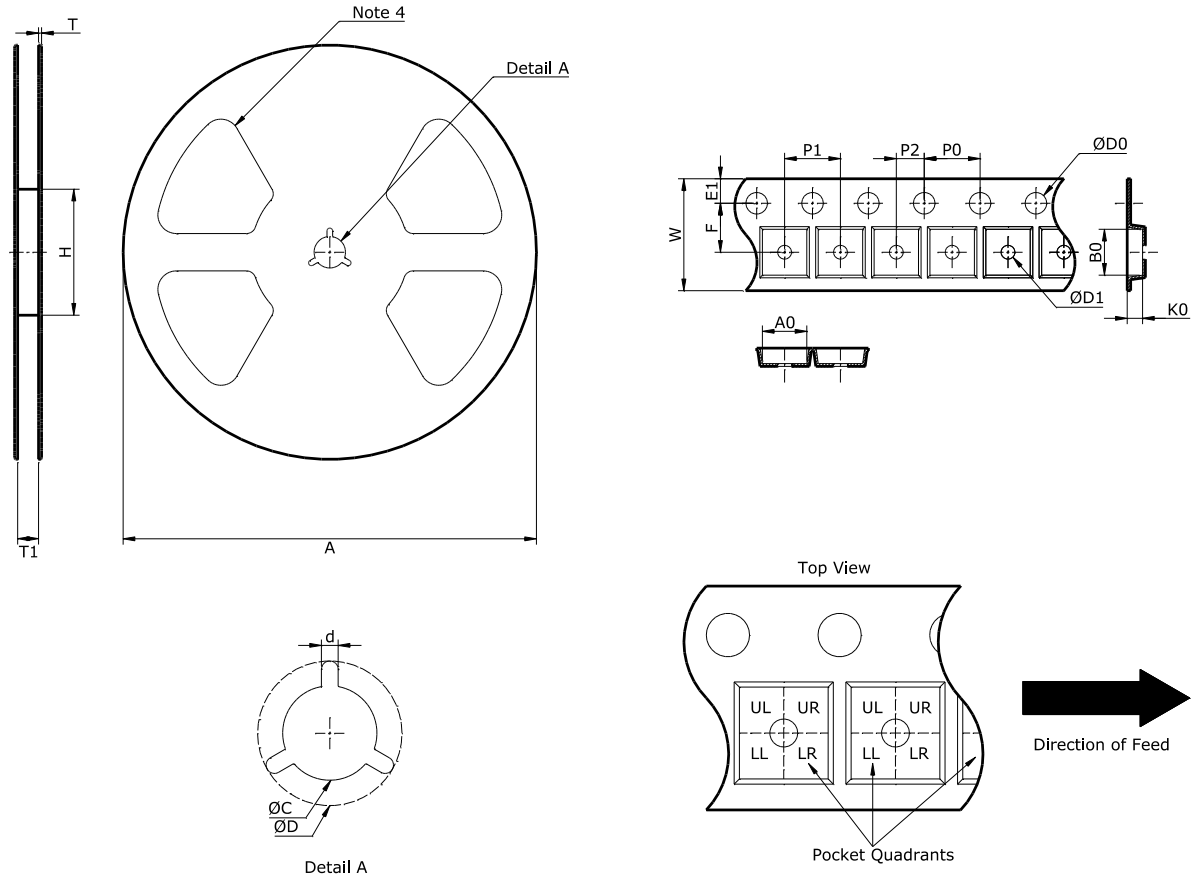

| Size / Symbol | Min. (mm) | Max. (mm) | Size / Symbol | Min. (mm) | Max. (mm) |
|---|---|---|---|---|---|
| A | 1.350 | 1.750 | E | 5.800 | 6.200 |
| A1 | 0.100 | 0.250 | E1 | 3.800 | 4.000 |
| A2 | 1.350 | 1.550 | e | 1.000(TYP) | |
| b | 0.330 | 0.510 | L | 0.400 | 1.270 |
| C | 0.170 | 0.250 | θ | 0 | 8° |
| D | 4.70 | 5.100 | | | |

| Top mark | Package |
|---|---|
| PN<br>PN8085/L/H<br>YWWXXXXX | SSOP10 |

Note: Y:Year Code; WW：Week Code; XXXXX: Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

## Tape and Reel Information




| SSOP10 Package | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **A (mm)** | **T (mm)** | **T1 (mm)** | **H (mm)** | **ØC (mm)** | **ØD (mm)** | **d (mm)** | **A0 (mm)** | **B0 (mm)** | **K0 (mm)** |
| 330 ±1.0 | 2.6 +1/−0 | 12.4 +1/−0 | 100 ±0.5 | 12.00 +0.5/−0.2 | 17.70 ±0.40 | 1.9 ±0.40 | 6.4 ±0.1 | 5.4 ±0.1 | 2.1 ±0.1 |
| **W (mm)** | **F (mm)** | **E1 (mm)** | **P0 (mm)** | **P1 (mm)** | **P2 (mm)** | **ØD0 (mm)** | **ØD1 (mm)** | **Pin 1 Quadrant** | |
| 12.00 ±0.3 | 5.50 ±0.1 | 1.75 ±0.10 | 4.00 ±0.10 | 8.0 ±0.1 | 2.0 ±0.05 | 1.5 +0.1/−0 | 1.55 +0.25/0 | UL | |

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

## Important Notice

Wuxi Chipown Microelectronics Co. Ltd. reserves the right to make changes without further notice to any products or specifications herein. Wuxi Chipown Microelectronics Co. Ltd. does not assume any responsibility for use of any its products for any particular purpose, nor does Wuxi Chipown Microelectronics Co. Ltd assume any liability arising out of the application or use of any its products or circuits. Wuxi Chipown Microelectronics Co. Ltd does not convey any license under its patent rights or other rights nor the rights of others.